(19) Europäisches Patentamt
European Patent Office
Office européen des brevets

(11) Publication number : **0 465 961 B1**

(12) # EUROPEAN PATENT SPECIFICATION

(45) Date of publication of patent specification : **09.08.95 Bulletin 95/32**

(51) Int. Cl.[6] : **H01L 29/772**

(21) Application number : **91110795.1**

(22) Date of filing : **28.06.91**

(54) **Semiconductor device on a dielectric isolated substrate.**

(30) Priority : **09.07.90 JP 180898/90**
**09.07.90 JP 180899/90**

(43) Date of publication of application :
**15.01.92 Bulletin 92/03**

(45) Publication of the grant of the patent :
**09.08.95 Bulletin 95/32**

(84) Designated Contracting States :
**DE FR GB**

(56) References cited :
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**EP 0 465 961 B1**

which results in losing an advantage of the MISFET utilizing the SOI substrate that the carrier mobility can be enhanced.

The MISFET structure 18 of Fig. 4 is advantageous with regard to an easier manufacturing process. Again, similar as in Fig. 3, the MISFET 18 shown in Fig. 4 is provided with a semiconductor region 16 of the same conductivity type as a channel region 12 formed outside and adjacent to a shallow source region 5. A common source electrode 9 is used, thereby making it possible to use the MISFET 18 as an ordinary three-terminal element. The positive holes h produced by the impact ionization are removed through the semiconductor region 16 and the source electrode 9 and the drain breakdown voltage is improved. However, as shown in Fig. 5, if a semiconductor region 19 of the same conductivity type as the semiconductor region 16 is additionally provided outside of the drain region 6 in consideration of a symmetric element structure of the MISFET 18, positive holes h from the semiconductor region 19 to the channel region 12 flow into the semiconductor region 16 on the side of the source region 15 (indicated by a hole current $I_{pp}$ in Fig. 5) causing problems with shortcircuiting, i. e. a more or less conducting state between the source and the drain, for example, under a non-operative condition. It is therefore impossible to apply this structure to a switching element such as an access transistor for a static RAM (random access memory) cell which uses the source and the drain alternately, so that the applicable range as a circuit element is limited.

## OBJECTS AND SUMMARY OF THE INVENTION

It is an object of the invention to provide an improved MIS-type semiconductor device in which the aforementioned shortcomings and disadvantages encountered with the prior art can be substantially eliminated.

More specifically, it is an object of the invention to provide a MIS-type semiconductor device in which degradation of the breakdown voltage due to impact ionization can be suppressed to thereby improve reliability of the semiconductor device itself.

It is another object of the invention to provide a MIS-type semiconductor device which can be applied to a wider variety of fields as a circuit element.

The semiconductor device of the present invention comprises the features of appended claim 1. According to the invention, the second conductivity type semiconductor region separated from the channel region is provided adjacent to the first conductivity type source region, such that the distance (width) $W_N$ of the source region between the second conductivity type semiconductor region and the channel region becomes shorter than the diffusion length $L_p$ of the minority carriers in the source region to thereby reduce the effective diffusion length of the minority carriers in the source region. Simultaneously, a bipolar transistor structure is formed by the second conductivity type channel region, the first conductivity type source region and the second conductivity type semiconductor region. Accordingly, if a predetermined potential voltage is applied to this second conductivity type semiconductor region or if the second conductivity type semiconductor region and the source region are connected in common, the channel region, the source region and the second conductivity type semiconductor region act as a bipolar transistor, thereby making it possible to remove a minority carrier current through the first conductivity type source region and the second conductivity type semiconductor region (e. g., a hole current if a n-channel MISFET is concerned) generated in the channel region due to the said impact ionization.

Therefore it is possible to prevent, on the one hand, the degradation of the breakdown voltage between the source and the drain while maintaining the advantages of the MISFET with a SOI substrate and, on the other hand, inhibiting shortcircuiting and conduction if the element structure is symmetric, which results in improved reliability of the semiconductor device and an enhanced applicable range as a circuit element.

The above and other objects, features and advantages of the present invention will become apparent from the following detailed description of illustrative embodiments thereof to be read in conjunction with the accompanying drawings, in which like reference numerals are used to identify the same or similar parts in the several view.

## BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a schematic diagram showing a structure of a first example of a MIS-type semiconductor device according to the prior art;

FIG. 2 is a schematic diagram showing a structure of a second example of a known MIS-type semiconductor device;

FIG. 3 is a schematic diagram showing a structure of a third example of a prior art MIS-type semiconductor device;

FIG. 4 is a schematic diagram showing the structure of a fourth example of a MIS-type semiconductor device according to the state of the art;

FIG. 5 is a schematic diagram of the structure of a fifth example of a MIS-type semiconductor device according to the prior art;

FIG. 6 is a schematic diagram of the structure of a first embodiment of a MIS-type semiconductor device according to the first concept of the invention;

FIG. 7 depicts a schematic diagram of the structure of a second modified embodiment of the first

plain another manufacturing process of the thirteenth embodiment of the invention, respectively.

## DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

The invention will now be described with reference to the drawings as applied to an n-channel MISFET in the respective embodiments. However, when reading the present disclosure, the person skilled in the art can of course readily transfer the ideas of the present invention to a p-channel MISFET.

Fig. 6 shows a first embodiment of the present invention which employs a SOI substrate 24 comprising a silicon thin film 23 insulatively formed on a silicon substrate 21 through a $SiO_2$ film 22. Within the p-type silicon thin film 23 comprised in the SOI substrate 24, a first conductivity type or n-type source region 25 and a drain region 26 are formed so as to reach the bottom of the $SiO_2$ film 22. A p-type region 28 whose conductivity type is opposite to that of the source region 25, is provided outside and adjacent to the source region 25 but separated and remote from a channel region 27. The distance (width) $W_N$ of the source region 25 between the p-type region 28 and the channel region 27 is selected to be shorter than the diffusion length $L_p$ of the minority carriers or positive holes in the source region 25. A gate electrode 30 made of, for example, polycrystalline silicon, is provided on the channel region 27 between the source region 25 and the drain region 26 through a gate insulating film 29 of, for example, $SiO_2$ or the like. Then, a source electrode 31, a drain electrode 32 and a lead-out electrode 33 are formed on the source region 25, the drain region 26 and the p-type region 28, respectively, to constitute a n-channel MISFET 34.

Figs. 7 to 9 show other embodiments of the invention which are respectively modified examples of Fig. 6. As shown in Fig. 7, the n-type source region 25 and the drain region 26 are formed so as to reach the $SiO_2$ film 22 at the bottom of the film 23 and the p-type region 28 is located in the n-type source region 25. As shown in Fig. 8, the n-type source region 25 and the drain region 26 have a depth which does not reach the $SiO_2$ film 22 at the bottom of the film 23, and the p-type region 28 is again located in the n-type source region 25. Further, as shows the plan view of Fig. 9, the p-type region 28 can also be formed in a portion surrounded by the n-type source region 26.

A predetermined voltage, for example ground voltage, is applied to the lead-out electrode 33 on the p-type region 28 of the respective MISFETs 34 to 37 shown in Figs. 6 through 9.

According to the structure described above, the p-type region 28 is provided adjacent or within the n-type source region 25 so as to be separated from the p-type channel region 27, whereby a pnp bipolar transistor structure is formed by the p-type channel region 27, the n-type source region 25 and the p-type region 28 serving as the emitter, the base and the collector, respectively. By this structure, holes h (hole current $L_p$) or the minority carriers generated by impact ionization occurring at the end of the drain region are released from the channel region 27 through the source region 25 and the p-type region 28 of the electrode 33, thereby making it possible to suppress the degradation of the breakdown voltage between the source and the drain due to the impact ionization.

While the MISFET devices are four-terminal elements in the above-described embodiments, they can be used as three-terminal elements by connecting the source region 25 and the p-type region 28 with an electrode metal or the like outside the device.

Fig. 10 shows a fifth embodiment of a three-terminal MISFET using the structure of Fig. 6, wherein a source electrode 31 partly covers both, the source region 25 and the p-type region 28 so as to commonly connect them with each other. Fig. 31 shows the simulation result of the characteristic of the source-drain breakdown voltage of the three-terminal MISFET 38 of Fig. 10. A curve II in Fig. 31 indicates the characteristic of the MISFET 38 of the fifth embodiment and a curve I in Fig. 31 the characteristic of the conventional MISFET shown in Fig. 1. Either of the samples has a p-type channel region in an impurity concentration of $5 \times 10^{15}$ $cm^{-3}$, and n-type source region and drain region in an impurity concentration of $1 \times 10^{20}$ $cm^{-3}$. The impurity concentration of the p-type region 28 of the fifth embodiment is $1 \times 10^{18}$ $cm^{-3}$. It is also assumed that the silicon thin film has a thickness of 100 nm and the $SiO_2$ film (on the bottom) of the SOI substrate has thickness of 1 µm $n^+$ polycrystalline silicon is used for the gate electrode, and a gate voltage $V_g$ is selected to be -0.5V.

It results from this simulation that the MISFET 38 of the fifth embodiment (Fig. 10) has an improved breakdown voltage between the source and the drain as compared with the conventional MISFET 11 (Fig. 1).

In the structure of the above-mentioned embodiments shown in Figs. 6 to 10, it is possible to place the n-type region 28 symmetrically adjacent to both sides of the source region 25 and the drain region 26. Fig. 11 shows as a sixth embodiment a MISFET of such type with a three-terminal LDD (lightly doped drain) structure.

This MISFET 39 has p-type regions 28A and 28B, respectively formed outside of a source region 25 and a drain region 26 having high concentration regions 25a, 26a and low concentration regions 25b, 26b, wherein the source region 25 and the p-type region 28A are commonly connected by the source electrode 31, and the drain region 26 and the p-type region 28B are commonly connected by the drain electrode 32. Also in this structure, the effective distance (width)

region 26 via a gate insulating film 29 made of, for example, $SiO_2$ or the like. Also, a source electrode 31, a drain electrode 32 and a lead-out electrode 48 are formed on the source region 25, the drain region 26 and the p-type region 47, respectively, to constitute a MISFET 49. The potential of the p-type region 47 may not coincide with the drain potential but must coincide with the source potential or must become substantially equal to the source potential. That is, as shown in a potential diagram of Fig. 34A (i. e., potential diagram along line X - X on the structure of Fig. 34B), a potential $p_b$ of the p-type region 47 must be selected to be lower than a potential $p_a$ of the channel region 27.

In the thus constructed MISFET 49, the p-type region 47 is formed on the side of the drain region 26 close to the source of electron-positive hole couplings generated by the impact ionization, whereby the positive holes h generated by the impact ionization can be released from the drain region 26 through the p-type region 47, which leads to the improvement of the breakdown voltage between the source and the drain. Fig. 33 shows results of simulation of the source-drain breakdown voltage characteristics of the MISFET 49 of the eleventh embodiment of the invention. In Fig. 33, a curve IV indicates the characteristic of the MISFET 49 of the eleventh embodiment, a curve I indicates the characteristic of the conventional MISFET 11 of Fig. 1 and a curve II indicates the characteristic of the MISFET 34 of Fig. 6. Test samples of the eleventh embodiment are essentially the same as those of Fig. 31 except that the impurity concentration of the p-type region 47 is selected to be $1 \times 10^{18}$ $cm^{-3}$ and that the potential of the p-type region 47 is selected to be 0 V which is similar to the potential of the source region. The results of simulation demonstrate that the source-drain breakdown voltage of the MISFET 49 of the eleventh embodiment is improved as compared with that of the conventional MISFET 11 of Fig. 1.

The structure of the MISFET 49 can achieve similar effects as those of the MISFET 34 of Fig. 6 except that it cannot be formed as a three-terminal structure.

Fig. 17 shows the eleventh embodiment of the present invention. In this eleventh embodiment, in a silicon thin film 23, for example, of p-type, comprised in an SOI substrate 24, there are formed a n-type source region 25 and a drain region 26, respectively, having high concentration regions 25a and 26a and low concentration regions 25c and 26c, formed beneath the high concentration regions 25a and 26a, reaching an $SiO_2$ film 22 at the bottom, respectively, and a p-type region 28 is formed adjacent to the high concentration region 25a and the low concentration region 25c of the source region 25 so as to be separated from a channel region 27. On the channel region 27 between the source region 25 and the drain region 26, there is formed a gate electrode 30 made, for example, of polycrystalline silicon through a gate insulating film 29 made of $SiO_2$ or the like, a source electrode 31 commonly connected, for example, to the p-type region 28 and the high concentration region 25a of the source region 25 is formed, and a drain electrode 32 is also formed on the high concentration region 26a of the drain region 26 to constitute a MISFET 51. The high concentration regions 25a and 26a are provided to reduce the source resistance and the drain resistance, respectively, while the low concentration region 25c is provided to allow a hole current generated by impact ionization, which will be described later, to readily flow to the p-type region 28. The width $W_N$ of the low concentration region 25c is selected to be shorter than the diffusion length Lp of the positive holes of the minority carriers.

The above-mentioned structure can be operated as a pnp bipolar transistor in which the p-type channel region 27, the low concentration region 25c of the n-type source region 25 and the p-type region 28 are respectively functioning as emitter, base and collector, whereby the holes h (hole current $I_p$) of the minority carriers generated by the impact ionization are released from the channel region 27 through the p-type region 28 to the source electrode 31 to suppress a degradation of the breakdown voltage between the source and the drain due to the impact ionization similarly to Fig. 6. Moreover, this embodiment provides the low concentration region 25c which further facilitates the flow of the positive holes as compared with Fig. 6, thereby making it possible to further improve the source-drain breakdown voltage.

Assuming that a channel current of the MISFET using the SOI substrate is $I_c$, a hole current generated in a high electric field is $I_p$ and an electron current provided when a channel potential becomes higher than a source potential to allow the bipolar operation is $I_n$, then a drain current $I_D$ is given by:

$$I_D = I_c + I_n + I_p \quad (1)$$

Further, assuming that a ratio in which the hole current $I_p$ is generated by the channel current $I_c$ and the electron current $I_n$ is $K(V_D)$, then we have:

$$I_p = K(V_D)\,(I_c + I_n) \quad (2)$$

Further, $I_p$ and $I_n$ may be transformed as follows:

$$I_p = S(qDpn_i^2/N_DW_N)(e^{\frac{qU}{kT}} - 1) \quad (3)$$

$$I_n = S(qDnn_i^2/N_A \cdot L)(e^{\frac{qU}{kT}} - 1) \quad (4)$$

where $D_p$ is the diffusion coefficient of the hole, S is the junction dimension, $n_i$ is the intrinsic carrier concentration, $N_D$ is the donor concentration in the low concentration region 25c of the source, $W_N$ is the width of the low concentration region 25c of the source, $N_A$ is the acceptor concentration in the channel region 27, L is the length of the channel region 27 and V is the potential difference between the source and the channel.

The above equations (1) to (4) yield:

tact windows 55 are respectively opened through a photoresist, and then a source electrode 31, a drain electrode 32 and a gate lead-out electrode 30A, all made of Al, are formed, for example, through a barrier metal, if necessary, to obtain a target MISFET 59.

According to the thus constructed MISFET 59, since the p-type region 28A and the source region 25, and the p-type region 28B and the drain region 26 are connected with each other by the Ti silicide film 58, a contact window of a minimum pattern, which is determined by the resolution of the photoresist, is sufficient for providing the window aperture 55 for a subsequently formed Al contact whereby the minimum dimension of the contact window 55 is reduced as compared with the fourteenth embodiment of Fig. 30. Therefore, the semiconductor device of this embodiment can be produced with fine pattern elements and is thus suitable to be incorporated into a highly-integrated device.

Since the aforementioned structure of Fig. 6 can be formed of a silicon thin film 23 with relatively thin thickness, a short channel effect is not likely to occur. However, in the structure having the low concentration regions 25c and 26c as shown in Fig. 17, the thickness of the silicon thin film 23 is increased so that the short channel effect occurs because it becomes difficult to control the semiconductor device by the gate voltage. There is then the risk that a leak current will increase. Accordingly, the concentration of the channel region 27 must be increased in order to avoid the short channel effect.

When the gate electrode 30 is made of phosphor-doped polycrystalline silicon, the channel concentration, particularly, the concentration on the surface of the channel is increased in order to control a threshold voltage $V_{th}$. By way of example, as described above with reference to Fig. 18, the concentration of the channel region 27 is selected to be about $10^{17}$ $cm^{-3}$ which is higher than that of the low concentration regions 25c and 26c of the source region and the drain region (approximately in a range of from $10^{15}$ $cm^{-3}$ to $10^{18}$ $cm^{-3}$). It is difficult to manufacture, by the prior art technique, the MISFET 52 shown in Fig. 18 which has a concentration lower than the channel region 27. Figs. 38A to 38D and Figs. 41A to 41H show examples of manufacturing process of the MISFET 52.

The example of Figs. 38A to 38D will first be described. Referring to Fig. 38A, a gate electrode 30 made of phosphor-doped polycrystalline silicon is formed on a silicon thin film 23 through a gate insulating film 29, and LDD-structured n-type low concentration regions 25b and 26b are formed with the gate electrode 30 used as a mask.

Next, side walls 61 made of SiO2 are formed on sides of the gate electrode 30, as shown in Fig. 38B, and then a p-type impurity, for example, boron 64 is ion-implanted so as to provide the channel region with a concentration of approximately $10^{17}$ $cm^{-3}$ (for example, not less than $10^{17}$ $cm^{-3}$ on the bottom and approximately $5 \times 10^{16}$ $cm^{-3}$ on the surface). This ion implantation is intended to control the threshold voltage $V_{th}$ as well as prevent the short channel effect. This ion implantation is performed through the gate electrode 30 to achieve a concentration profile such that an ion implantation peak 64 exists in the vicinity of the bottom of the channel 27.

Fig. 39A shows a concentration profile on a line A-A passing the channel region 27 after the ion implantation and active anneal processing, wherein reference numeral 62 designates a concentration profile of boron, and 63 that of the gate electrode 30 made of $n^+$ polycrystalline silicon. Thus, portions corresponding to the source region 25 and the drain region 26 are lower by the thickness of the gate electrode 30, whereby an ion implantation peak $64_2$ exists in the $SiO_2$ film 22 positioned beneath the source and drain regions, so that the boron concentration is extremely low. More specifically, it is lower than the concentration in the n-type low concentration regions 25c, 26c formed in the later process. Fig. 39B shows a concentration profile on a line B-B passing the source region 25 (or the drain region 26), wherein reference numeral 62 designates a concentration profile of boron. Reference numeral 65 designates a concentration profile of the high concentration region 25a (or 26a) and the low concentration region 25c (or 26c) of the source region (or the drain region), later referred to.

Subsequently, an n-type impurity 66 in a low concentration is ion-implanted to form the n-type low concentration regions 25c, 26c in a concentration of approximately $10^{15}$ $cm^{-3}$ to $10^{18}$ $cm^{-3}$, and then a n-type impurity 67 in a high concentration is ion-implanted to form the high concentration regions 25a, 26a in a concentration of approximately $10^{20}$ $cm^{-3}$ on the n-type low concentration regions 25c and 26c, as shown in Fig. 38C. Thus, the source region 25 is composed of the regions 25a, 25b and 25c while the drain region 26 of the regions 26a, 26b and 26c.

Next, as shown in Fig. 38D, p-type impurity, for example, boron 69 is implanted through a photoresist mask 68 to form the p-type regions 28A and 28B outside the source region 25 and the drain region 26 but separated from the channel region 27. Then, a source electrode and a drain electrode are formed to obtain the MISFET 52 shown in Fig. 18. According to this manufacturing method, the boron 64 is implanted by utilizing the thickness of the gate electrode 30 to raise only the concentration of the channel region 27, so that the n-type low concentration regions 25c, 26c, in a concentration lower than that of the channel region 27 can be formed by the later ion implantation of the impurity 66. It is therefore possible to readily manufacture the MISFET 52 shown in Fig. 18 capable of preventing the short channel effect in a high accuracy and in a self-align fashion. It is also possible to readily

gion 26 to constitute an n-channel MISFET 94.

Figs. 20 through 22 show fifteenth to seventeenth embodiments which are respectively modified examples of Fig. 19. In Fig. 20, the n-type source region 25 and drain region 26 are formed so as to reach the $SiO_2$ film 22 on the bottom of the SOI substrate, and the metal layer 83 is formed within the n-type source region 25. In Fig. 21, the n-type source region 25 and drain region 26 are formed with a depth which does not reach the $SiO_2$ film 22 on the bottom of the SOI substrate, and the metal layer 83 is formed within the n-type source region 25. Further, in Fig. 22, the metal layer 83 is formed in a portion of the n-type source region 25, shown in a plane view. In either case, the metal layer 83 is constituted of an ohmic metal, and the distance $W_N$ of the source region 25 is selected to be shorter than the diffusion length $L_p$ of the positive hole.

When the positive holes of the electron-hole couplings generated by the impact ionization enter the source region 25, they flow toward the metal layer 83 by diffusion. Fig. 35 shows the dependence of a hole current Ip flowing through the metal layer 83 upon the distance (width) $W_N$ of the source region 25. A curve II in Fig. 35 indicates a diffusion current of the hole, a curve III in Fig. 35 indicates a recombination current, and a curve I in Fig. 35 indicates the effective hole current $I_p$ obtained as the sum of the diffusion current and the recombination current. The diffusion current is proportional to $1/W_N$, whereby as the the distance $W_N$ is increased beyond the diffusion length $L_p$ of the minority carrier (the positive hole in this case), the hole current Ip becomes constant (or equal to the recombination current).

Thus, according to the MISFET 94 of the present embodiment, the metal layer 83 ohmically contacted with the source region 25 is formed within the silicon thin film 23, and the distance $W_N$ of the source region 25 between the metal layer 83 and the channel region 27 is made shorter than the diffusion length $L_p$ of the positive hole or the minority carrier, whereby the hole current Ip caused by the picture holes generated by the impact ionization and flowing toward the metal layer 83 is increased, and as the result the degradation of the breakdown voltage between the source and the drain can be suppressed.

In the structures of the above-mentioned embodiments shown in Figs. 19 to 22, it is possible to place the metal layer 83 symmetrically adjacent-to both sides of the source region 25 and the drain region 26. Fig. 23 shows an example of a three-terminal LDD (Lightly doped drain) structure. This MISFET 98 has metal layers 83A and 83B respectively formed outside a source region 25 and a drain region 26 having high concentration regions 25a, 26a and low concentration regions 25b, 26b such that the metal layers are in ohmic contact with the corresponding source region 25 and drain region 26 but separated from a channel region 27. In this case, the effective distance $W_N$ of the symmetric source region 25 and drain region 26 are selected to be shorter than the diffusion length $L_p$ of the positive holes or the minority carrier. The metal layers 83A and 83B are used commonly as a source electrode and a drain electrode, respectively. Specifically, a gate electrode 30 is made, for example, of a boron-doped polycrystalline silicon, the thickness d of the silicon thin film 23 is selected to be 80 nm, the impurity concentration of the channel region 27 approximately $10^{14}$ $cm^{-3}$, the impurity concentration of the low concentration regions 25b and 26b of the source region and the drain region approximately $10^{17}$ $cm^{-3}$, and the impurity concentration of the high concentration regions 25a and 26a approximately $10^{20}$ $cm^{-3}$.

According to the MISFETs 94, 95, 96, 97 of the embodiments described above, it is possible to suppress the degradation of the breakdown voltage between the source and the drain due to the impact ionization. Further, since the metal layer 83 can be symmetrically formed on both sides of the source region 25 and the drain region 26, they can be used as a switching element such as an access transistor for a static RAM cell, thereby making it possible to extend an applicable range in circuit elements.

Also, the structure is simple because the metal layer 83 is merely formed outside the source region or outside the source region and the drain region, thereby providing a simple manufacturing process.

Further, the devices thus structured will not damage advantages of elements utilizing the SOI substrate such as a small parasitic capacitance, a large freedom in setting the impurity concentration in the channel region 27, and a high durability against $\alpha$ rays and latch-up.

In the nineteenth embodiment shown in Fig. 24, in a silicon thin film 23, for example, of p-type, comprised in an SOI substrate 24, there are formed n-type source region 25 and drain region 26 respectively having high concentration regions 25a and 26a and low concentration regions 25c and 26c, formed beneath the high concentration regions, reaching an $SiO_2$ film 22 on the bottom, and a metal layer 83 is formed adjacent to the high concentration region 25a and the low concentration region 25c of the source region 25 but separated from the channel region 27. The metal layer 83 is contacted with the high concentration region 25a in an ohmic fashion, while a Schottky junction is formed between the metal layer 83 and the low concentration region 25c. The distance $W_N$ of the low concentration region 25c of the source region between the metal layer 83 and the channel region 27 is selected to be shorter than the diffusion length $L_p$ of the positive holes. Then, on the channel region 27 between the source region 25 and the drain region 26, there is formed a gate electrode 30 made, for example, of polycrystalline silicon through a gate insulating

of the low concentration regions 25c and 26c approximately $10^{15}$ to $10^{16}$ $cm^{-3}$.

Since the source and drain can be symmetrically formed as described above, the element of the present embodiment can be used as a switching element such as an access transistor for a static RAM cell.

Figs. 26A through 26F show the twenty-first embodiment of the present invention which will be described with a manufacturing process thereof.

As shown in Fig. 26A, in this embodiment, a gate insulating film 29 made of $SiO_2$ or the like and a gate electrode 30 made of polycrystalline silicon are formed in a silicon thin film 23 comprised in an SOI substrate 24. Then, LDD-structured n-type source region 25 and drain region 26 having low concentration regions 25b, 26b and high concentration regions 25a, 26a are formed such that the source region 25 and the drain region 26 provide shallow junctions. Further, on the surfaces of the high concentration regions 25a and 26a of the source region and the drain region and the surface of the gate electrode 30, there are formed a silicide layers made of high melting point metal, for example, titanium silicide ($TiSi_2$) layer 100.

Next, as shown in Fig. 26B, an inter-layer insulating film 101 is formed and a window 102 for exposing a gate contact portion is formed. Then, as shown in Fig. 26C, windows 104 and 105 corresponding to a source contact portion and a drain contact portion, respectively, are formed through a photo-resist mask 103. Further, grooves 106 and 107 are formed by selectively etching the silicon portions through the windows 104 and 105 to a depth reaching the $SiO_2$ film 22 on the bottom of the film 23.

Next, as shown in Fig. 26D, an n-type impurity 108 of a low concentration is ion-implanted with a predetermined implanting angle to form n-type low concentration regions 25c and 26c reaching the $SiO_2$ film 22 on the bottom immediately beneath the high concentration regions 25a and 26b of the source region and the drain region. In this event, the width $W_1$ (corresponding to $W_N$) of the low concentration regions 25c and 26c is made sufficiently shorter than the diffusion length $L_p$ of the minority carrier ($W_N << L_p$). The width $W_1$ can be controlled by an implanting angle at the time of the ion implantation, an implanting energy, and a subsequent anneal processing.

Next, as shown in Fig. 26E, a film 109 made, for example, of Ti, which is a high melting point metal, is deposited on the inner surfaces of the grooves 106 and 107 and annealed to form titanium silicide ($TiSi_2$) films 110 on the inner walls of the grooves 106 and 107, that is, on the respective surfaces of the high concentration regions 25a, 26a and the low concentration regions 25c, 26c of the source region 25 and the drain region 26. The titanium silicide films 110 are ohmically contacted with the high concentration regions 25a, 26a and form Schottky junctions with the low concentration regions 25c, 26c.

Thereafter, as shown in Fig. 26F, Al films 112 are formed in the respective grooves 106 and 107 and on the gate electrode 30 through barrier metal, for example, TiON films 111, and then a source electrode 31, a drain electrode 32 and a gate lead-out electrode 113 are formed by the patterning-process, to thereby obtain a target MISFET 114. In this structure, metal layers 83A and 83B are composed of the titanium silicide films 110, the barrier metal films 111 and the Al films 112.

According to the thus constructed MISFET 114, it is possible to provide the n-type low concentration regions 25c, 26c sufficiently narrower than the diffusion length $L_p$ of the minority carrier ($W_N << L_p$) so that a hole current $I_p$ flowing to the metal layer 83A is increased. Simultaneously, by virtue of the Schottky junction formed between the metal layer 83A and the low concentration region 25c, a drift current based on an electric field prevailing at the Schottky junction is generated in addition to a diffusion current, whereby the hole current $I_p$ is further increased. It is therefore possible to further improve the breakdown voltage between the source and the drain as compared with the foregoing respective embodiments.

Also, in the manufacturing process, it is possible to form the low concentration region 25c in a remarkably narrow width. Further, the element of the present embodiment can be readily manufactured only by adding a process for forming the grooves 106 and 107.

Figs. 27A through 27E show the twenty-second embodiment which is a modified example of Figs. 26A through 26F. As shown in Fig. 27A, in this embodiment, in a silicon thin film 23 comprised in an SOI substrate 24 there are formed a gate insulating film 29, a gate electrode 30 made of polycrystalline silicon, n-type source region 25 and drain region 26 respectively composed of high concentration regions 25a, 26a and low concentration regions 25b, 26b. Further, for example, a titanium silicide film 100 is formed over the whole surfaces of the source region 25, the drain region 26 and the gate electrode 30.

Next, as shown in Fig. 27B, an inter-larger insulating film 101 is formed and at the same time, windows 102, 104 and 105 to which the gate contact portion, the source contact position and the drain contact portion of the inter-layer insulating film 101 faces, respectively are formed.

Next, as shown in Fig. 27C, n-type impurities 108 of a low concentration is ion-implanted with a predetermined implanting angle through an ion implanting mask, for example, a photo-resist mask 103 and windows 104, 105 to form n-type low concentration regions 25c, 26c reaching an $SiO_2$ film 22 on the bottom immediately beneath the high concentration regions 25a, 26a of the source region and the drain region. In this case, the width $d_2$ of the low concentration regions 25c, 26c is made wider than the width $d_1$ of the

wherein said source region and said drain region are formed with a depth which does not reach said insulating film on the bottom of said semiconductor layer.

6. The semiconductor device (39) according to claim 1 or 2, comprising a second lead-out region (28B) having the same conductivity type as said channel region and formed adjacent to said drain region but separated from said channel region.

7. The semiconductor device according to claim 6, wherein said source region has a low concentration source region (25b) between said channel region and a high concentration source region (25a), and said drain region has a low concentration drain region (26b) between said channel region and a high concentration drain region (26a).

8. The semiconductor device according to claim 1, wherein said lead-out region (28) is formed as a second semiconductor layer (41) on top of said source region (25).

9. The semiconductor device according to claim 8, wherein said second semiconductor layer (41) is made of monocrystalline silicon.

10. The semiconductor device according to claim 8, wherein said second semiconductor layer is made of polycrystalline silicon.

11. The semiconductor device according to claim 2, wherein said lead-out electrode (33) coincides with said source electrode (31) and/or said drain electrode (32), respectively.

12. The semiconductor device (51) according to claim 1 **characterized in that** said source region (25) comprises a high concentration source region (25a) and a low concentration source region (25c) formed beneath said high concentration source region, and said drain region comprises a high concentration drain region (26a) and a low concentration drain region (26c) formed beneath said high concentration drain region.

13. The semiconductor device (52) according to claim 12, **characterized in that** said high concentration source region (25a) is separated from said channel region by a first low concentration source region (25b), and in that said high concentration drain region (26a) is separated from said channel region by a first low concentration drain region (26b).

14. The semiconductor device according to claim 13, **characterized in that** a first lead-out region (28A) and a second lead-out region (28B) having the same conductivity type as said channel region are respectively formed adjacent to said source region and said drain region but respectively opposite to and separated from said channel region.

15. The semiconductor device according to claim 1, wherein said lead-out region is made of a refractory metal.

16. The semiconductor device according to claim 6, wherein both said first lead-out region and said second lead-out region are made of a refractory metal.

17. The semiconductor device according to claim 11, wherein said lead-out region is made of a refractory metal.

18. The semiconductor device according to claim 12, wherein said lead-out region is made of a refractory metal.

19. The semiconductor device according to claim 14, wherein both, said first lead-out region and said second lead-out region are made of a refractory metal.

20. The semiconductor device (59) according to claim 1 comprising a first lead-out region (28A) provided adjacent to said source region; **characterized in that** a second lead-out region (28B) being a part of said semiconductor layer (23) and having the same conductivity as said channel region is provided, wherein said source region (25) has a low concentration source region (25b) between said channel region (27) and a high concentration source region (25a), and said drain region (26) has a low concentration drain region (26b) between said channel region (27) and a high concentration drain region (26a), and said second lead-out region (28B) is formed adjacent to said drain region but opposite to and separated from said channel region; and in that a barrier metal (58) is formed on an area covering said high concentration source region and said first lead-out region and on an area covering said drain region and said second lead-out region.

21. A semiconductor device according to claim 20, wherein said gate electrode is also covered with barrier metal.

**Patentansprüche**

1. Halbleiter-Bauelement (34) mit:

sowohl der erste als auch der zweite Herausführbereich aus einem hochschmelzenden Metall bestehen.

17. Halbleiter-Bauelement nach Anspruch 11, bei dem der Herausführbereich aus einem hochschmelzenden Metall besteht.

18. Halbleiter-Bauelement nach Anspruch 12, bei dem der Herausführbereich aus einem hochschmelzenden Metall besteht.

19. Halbleiter-Bauelement nach Anspruch 14, bei dem sowohl der erste als auch der zweite Herausführbereich aus einem hochschmelzenden Metall bestehen.

20. Halbleiter-Bauelement (59) nach Anspruch 1, mit einem ersten Herausführbereich (28A), der angrenzend an den Sourcebereich vorhanden ist, **dadurch gekennzeichnet, daß** ein zweiter Herausführbereich (28B), der Teil der Halbleiterschicht (23) ist und denselben Leitungstyp wie der Kanalbereich aufweist, vorhanden ist, wobei der Sourcebereich (25) einen Sourcebereich (25b) mit niedriger Konzentration zwischen dem Kanalbereich (27) und einem Sourcebereich (25a) mit hoher Konzentration aufweist, und der Drainbereich (26) einen Drainbereich (26b) mit niedriger Konzentration zwischen dem Kanalbereich (27) und einem Drainbereich (26a) mit hoher Konzentration aufweist, und der zweite Herausführbereich (28B) angrenzend an den Drainbereich, jedoch abgewandt und getrennt vom Kanalbereich ausgebildet ist, und daß ein Sperrschichtmetall (58) auf einer den Sourcebereich mit hoher Konzentration und den ersten Herausführbereich abdeckenden Fläche und einer den Drainbereich und den zweiten Herausführbereich abdeckenden Fläche ausgebildet ist.

21. Halbleiter-Bauelement nach Anspruch 20, bei dem auch die Gateelektrode durch das Sperrschichtmetall abgedeckt ist.

## Revendications

1. Dispositif à semiconducteur (34) comprenant:

un substrat (21);

une couche isolante (22) formée sur ledit substrat (21);

une couche semiconductrice (23) munie d'une région de source (25) munie d'une électrode de source (31), d'une région de drain (26) munie d'une électrode de drain (32) et d'une région de canal (27);

une électrode de grille (30) formée sur ladite couche semiconductrice (23) au-dessus de ladite région de canal (27) au travers d'un film d'isolation de grille (29); et

une région de connexion de sortie (28) présentant le même type de conductivité que celui de ladite région de canal (27), munie d'une électrode de connexion de sortie (33),

caractérisé en ce que ladite région de connexion de sortie (28) est complètement séparée de ladite région de canal (27) par une région d'une conductivité opposée de telle sorte que la distance $W_N$ séparant ladite région de connexion de sortie (28) et ladite région de canal (27) soit plus courte que la longueur de diffusion $L_p$ des porteurs minoritaires de ladite région de canal (27).

2. Dispositif à semiconducteur selon la revendication 1, dans lequel ladite région de connexion de sortie (28) est prévue de manière à être adjacente à ladite région de source (25) et/ou à ladite région de drain (26) mais de manière à être opposée à ladite région de canal (27).

3. Dispositif à semiconducteur selon la revendication 1, dans lequel ladite région de source et ladite région de drain sont formées de manière à atteindre ladite couche isolante au niveau du fond de ladite couche semiconductrice.

4. Dispositif à semiconducteur selon la revendication 1, dans lequel la profondeur de ladite région de connexion de sortie est plus faible que la profondeur de ladite région de source.

5. Dispositif à semiconducteur selon la revendication 4, dans lequel ladite région de source et ladite région de drain sont formées moyennant une profondeur qui fait qu'elles n'atteignent pas ledit film d'isolation sur le fond de la couche semiconductrice.

6. Dispositif à semiconducteur (39) selon la revendication 1 ou 2, comprenant une seconde région de connexion de sortie (28B) présentant le même type de conductivité que celui de ladite région de canal et formée de manière à être adjacente à ladite région de drain mais de manière à être séparée de ladite région de canal.

7. Dispositif à semiconducteur selon la revendication 6, dans lequel ladite région de source comporte une région de source à faible concentration (25b) entre ladite région de canal et une région de source à haute concentration (25a) et ladite région de drain comporte une région de drain à faible concentration (26b) entre ladite région de canal et une région de drain à haute

FIG. 1

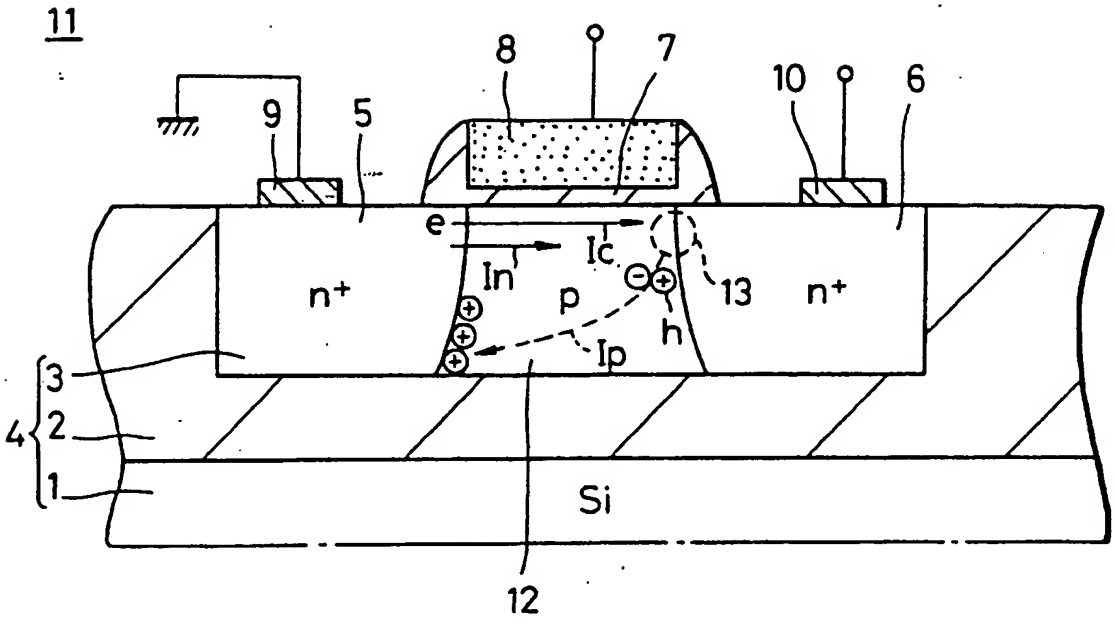



FIG. 2

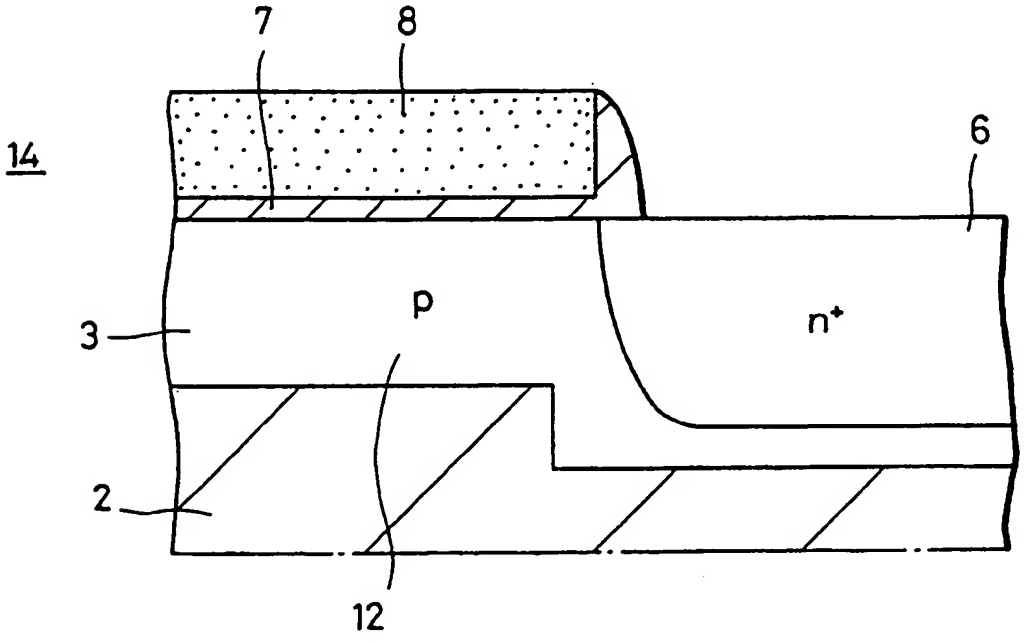


FIG. 5

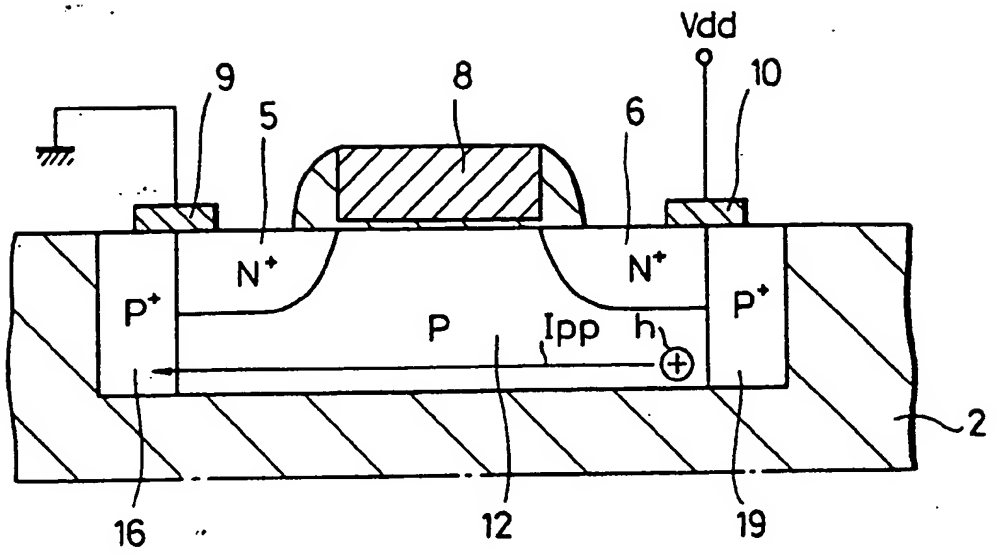

Vdd
9
8
10
5
6
N+
N+
P+
P+
P
Ipp
h
2
16
12
19

FIG. 6

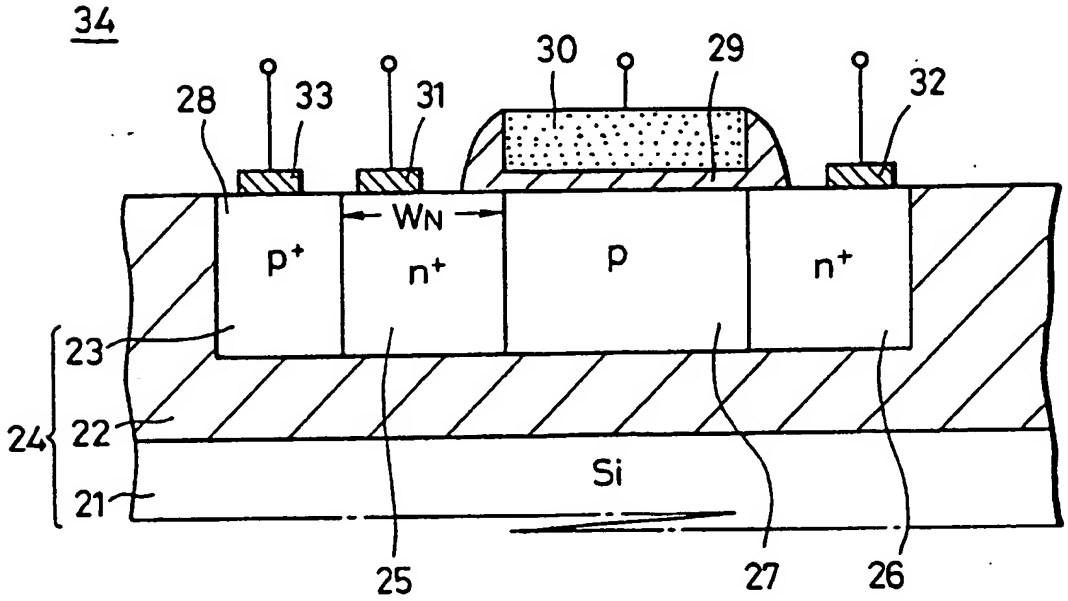

34
30
29
28
33
31
32
WN
p+
n+
P
n+
23
24
22
Si
21
25
27
26

FIG. 9

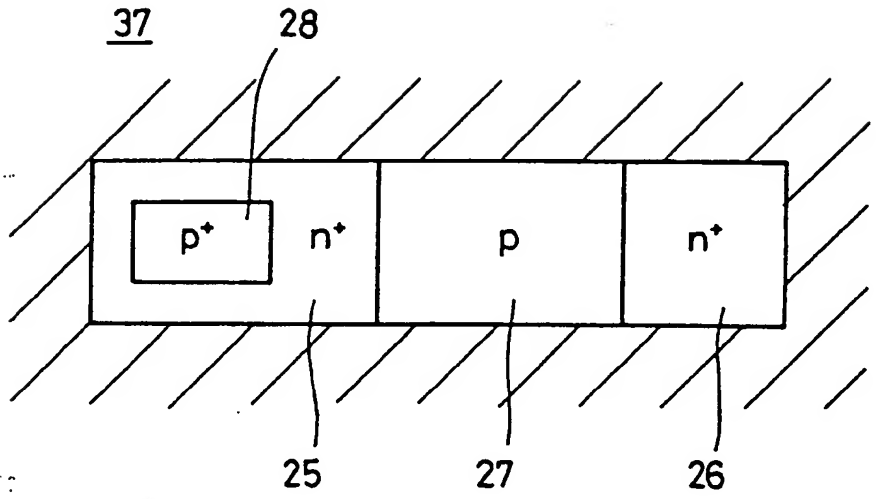



FIG. 10

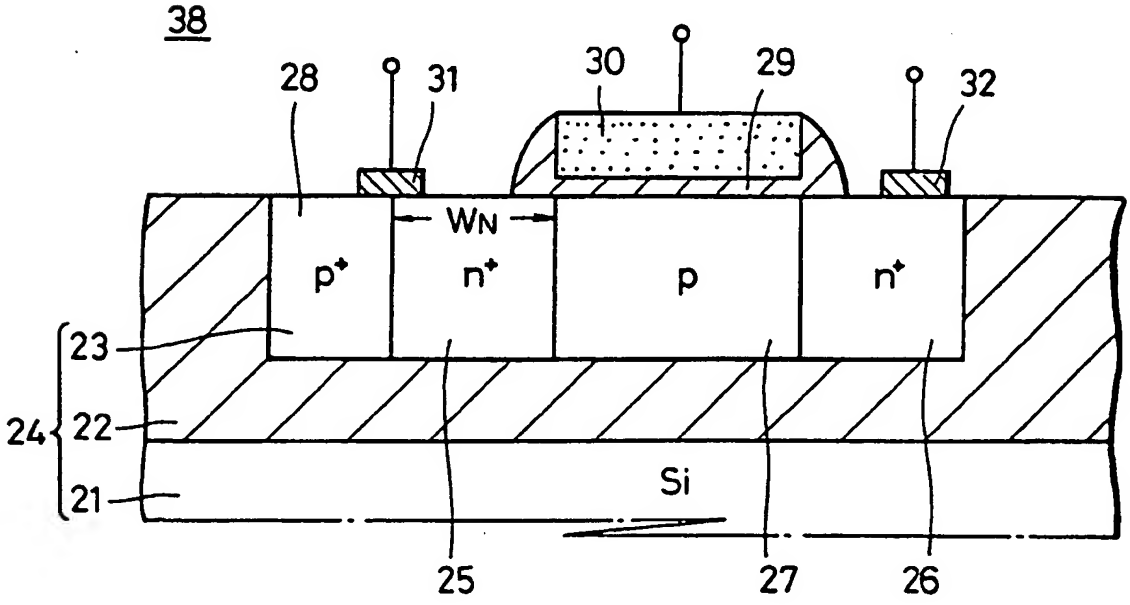


FIG. 13

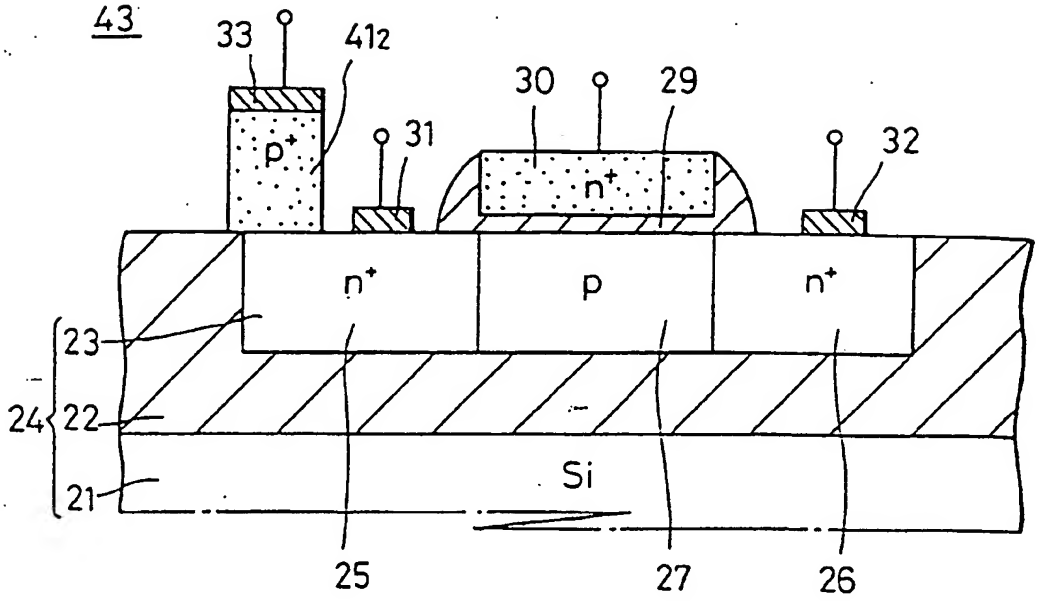

43
33
412
30
29
31
32
p+
n+
n+
p
n+
23
24
22
21
Si
25
27
26

FIG. 14

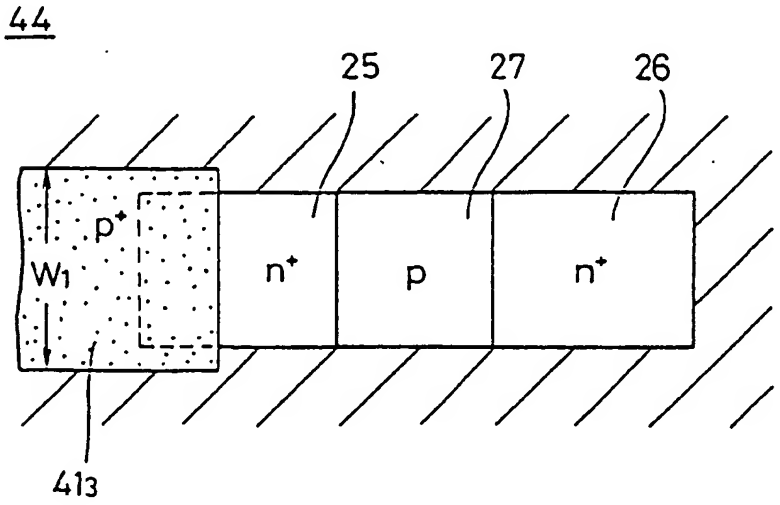

44
25
27
26
p+
W1
n+
p
n+
413

FIG. 17

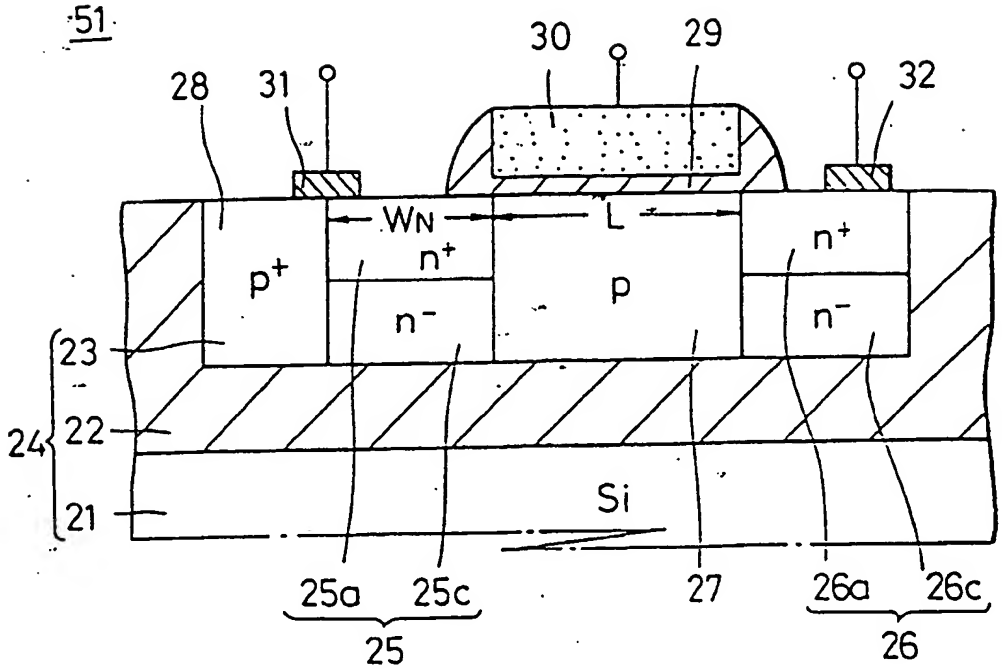
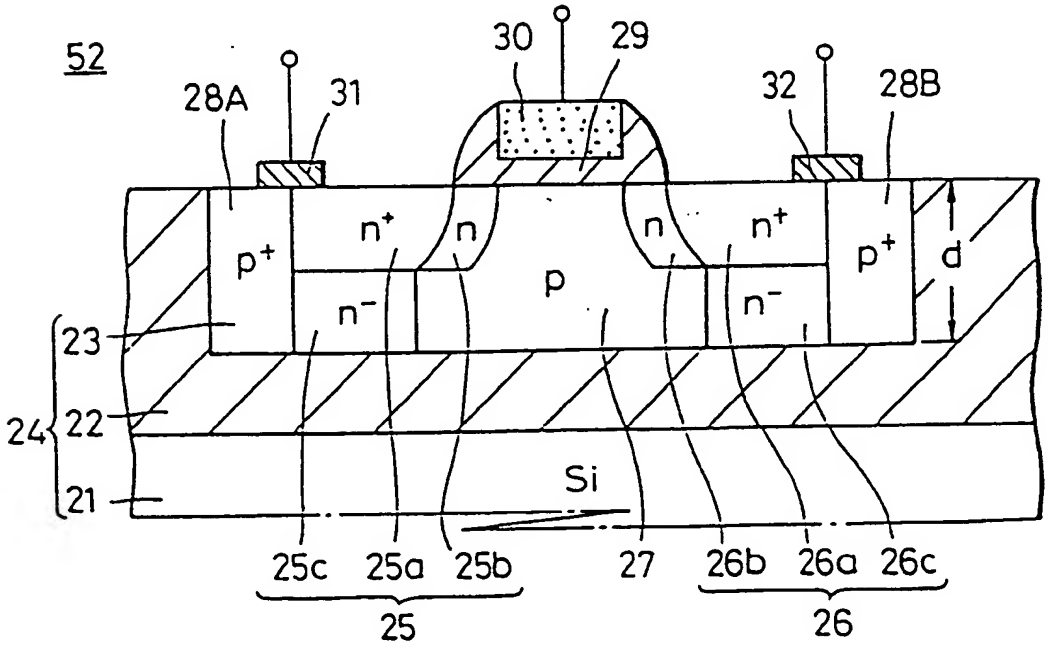

51
30
29
28
31
32
WN
L
n+
p+
n+
p
n−
n−
23
24
22
21
Si
25a
25c
27
26a
26c
25
26

FIG. 18


52
30
29
28A
31
32
28B
n+
n
n
n+
p+
p+
d
n−
p
n−
23
24
22
21
Si
25c
25a
25b
27
26b
26a
26c
25
26

96 FIG. 21

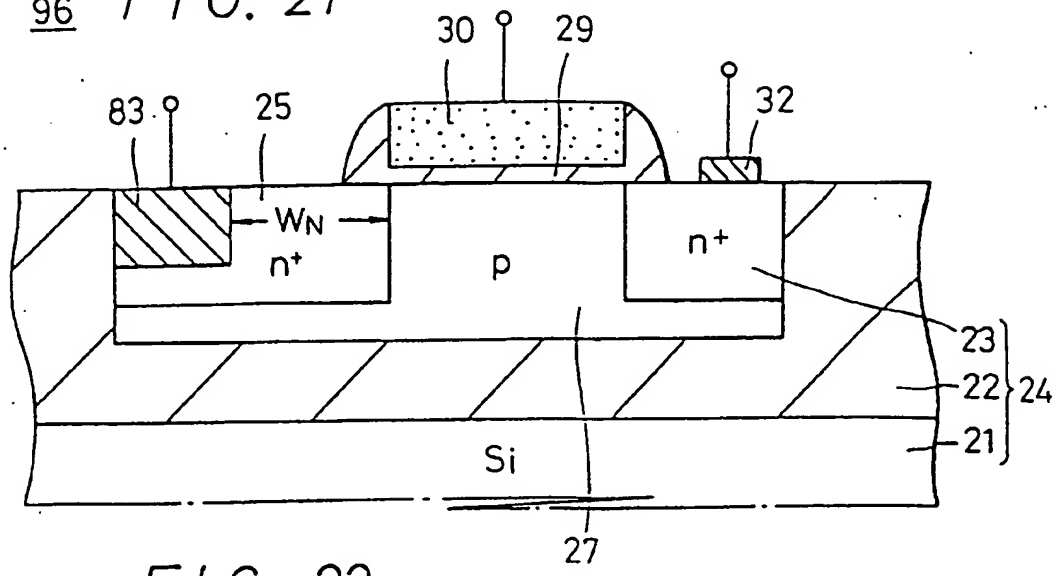



FIG. 22

97

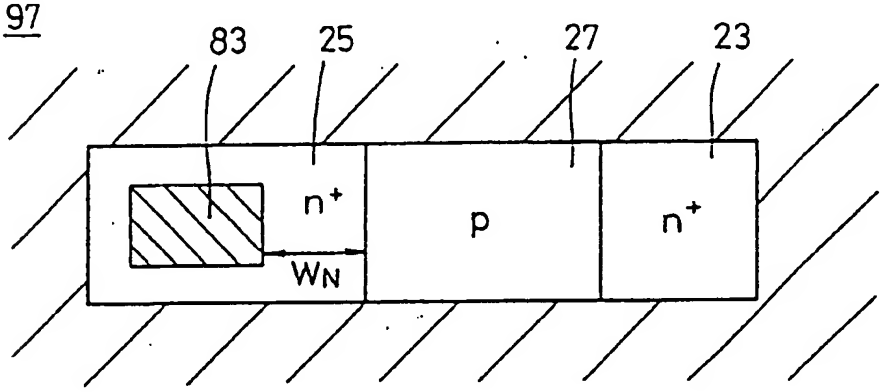
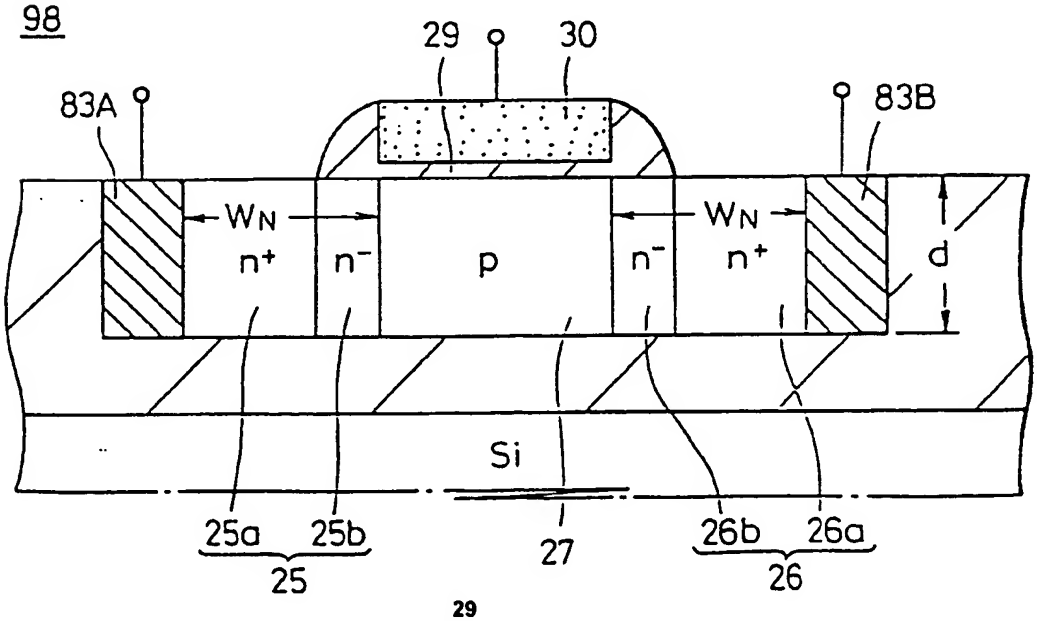



FIG. 23

98



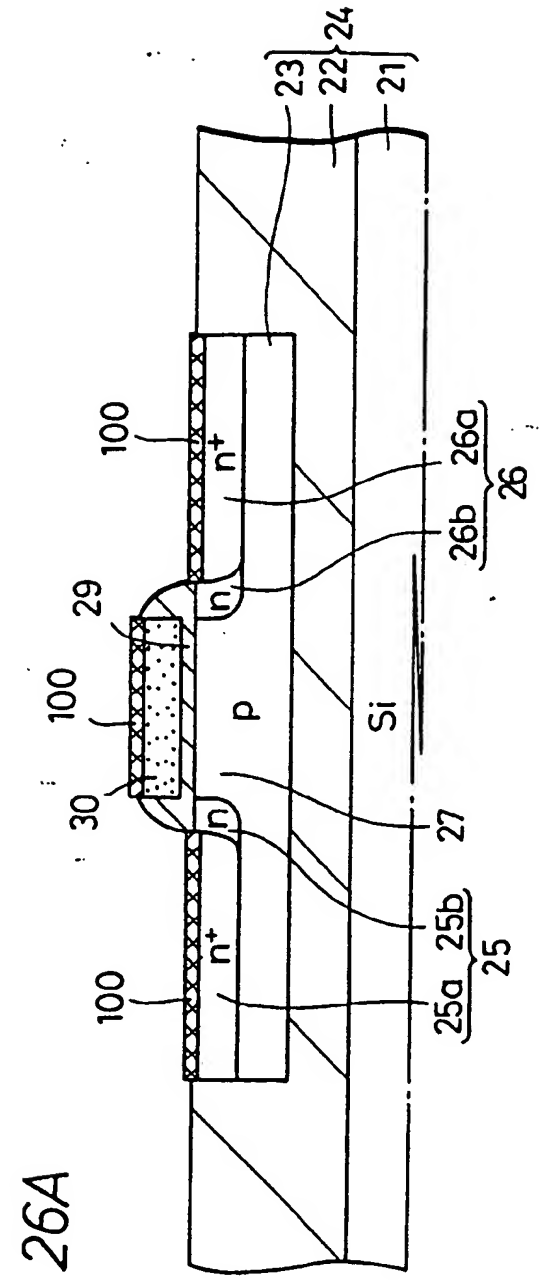



FIG. 26A

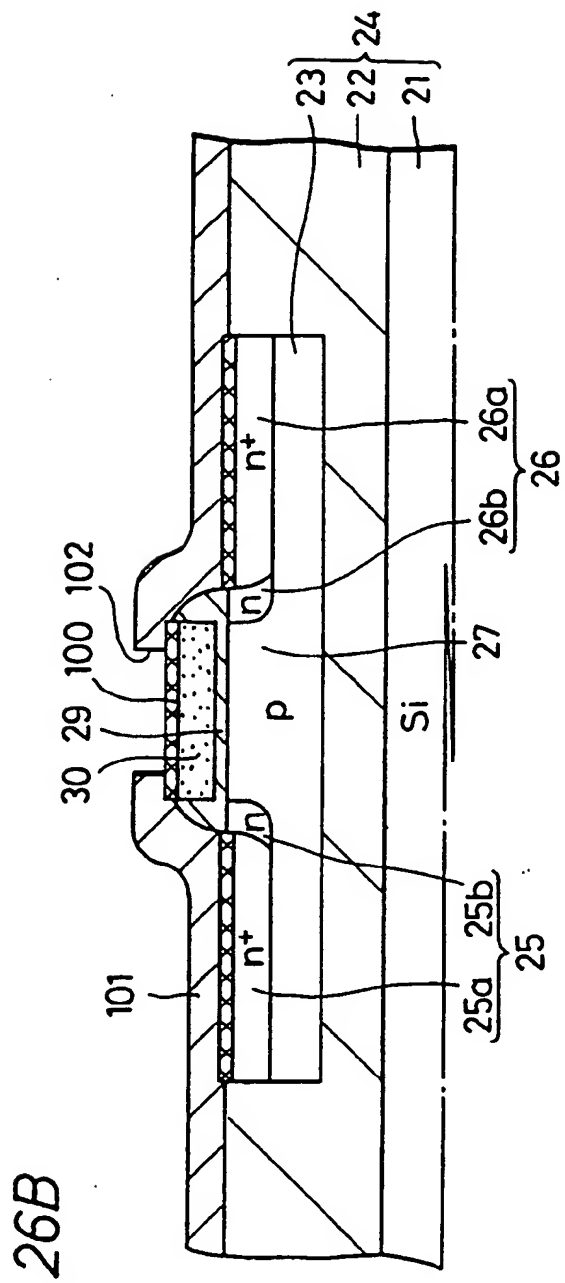



FIG. 26B

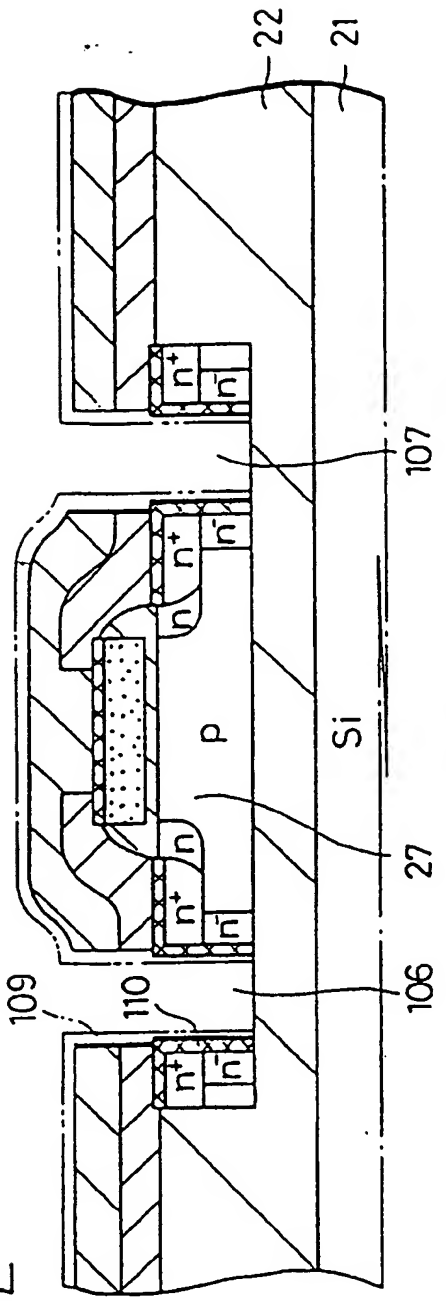



FIG. 26E

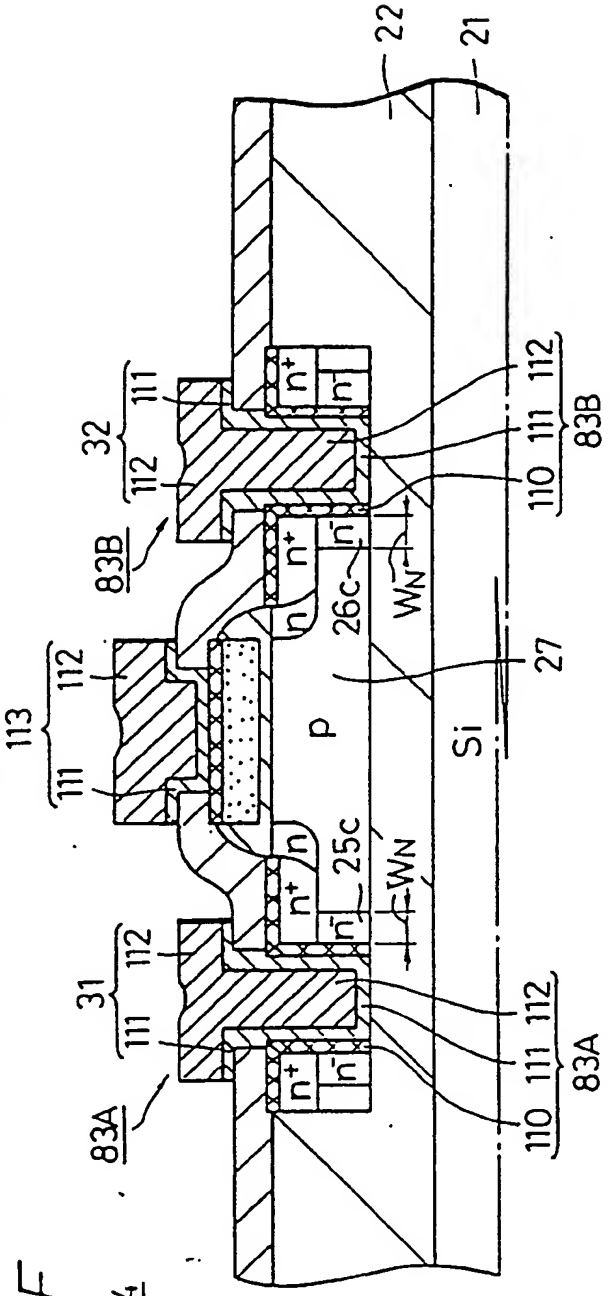



FIG. 26F

FIG. 27D

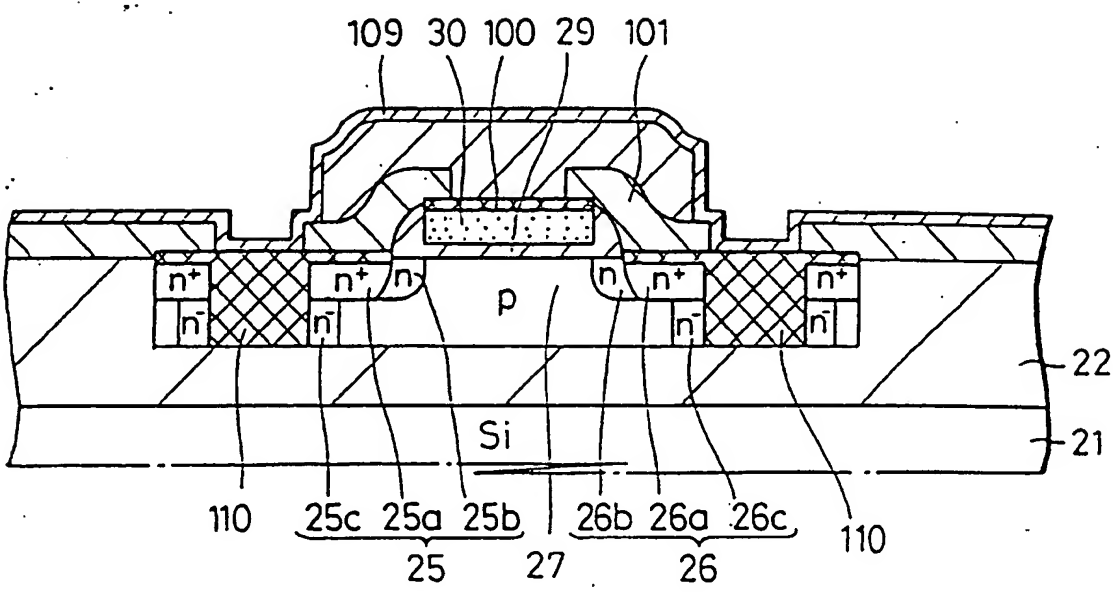



FIG. 27E

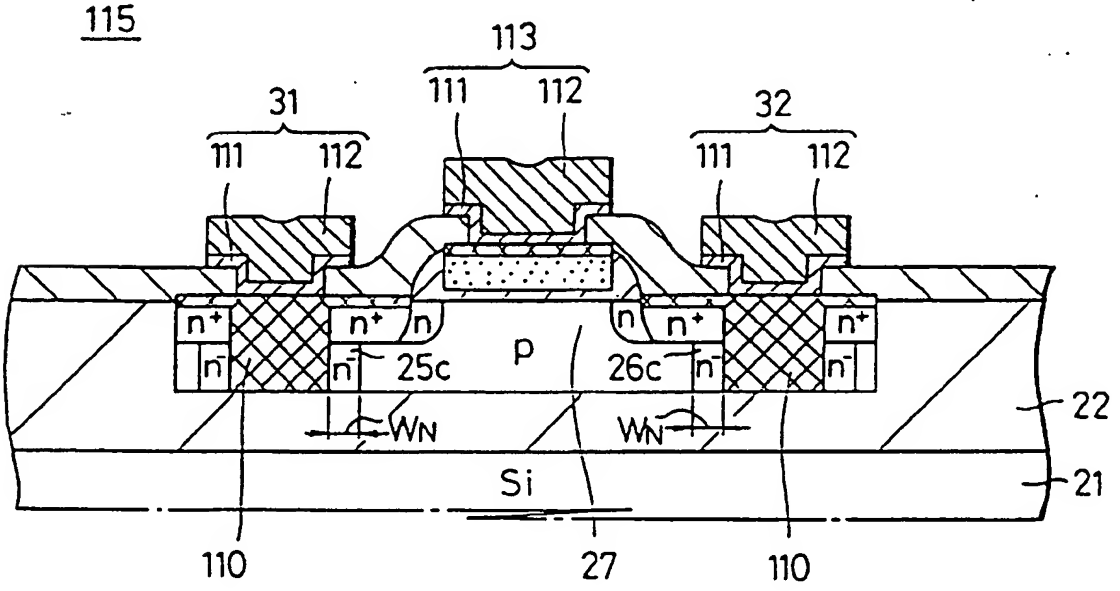


FIG. 29A

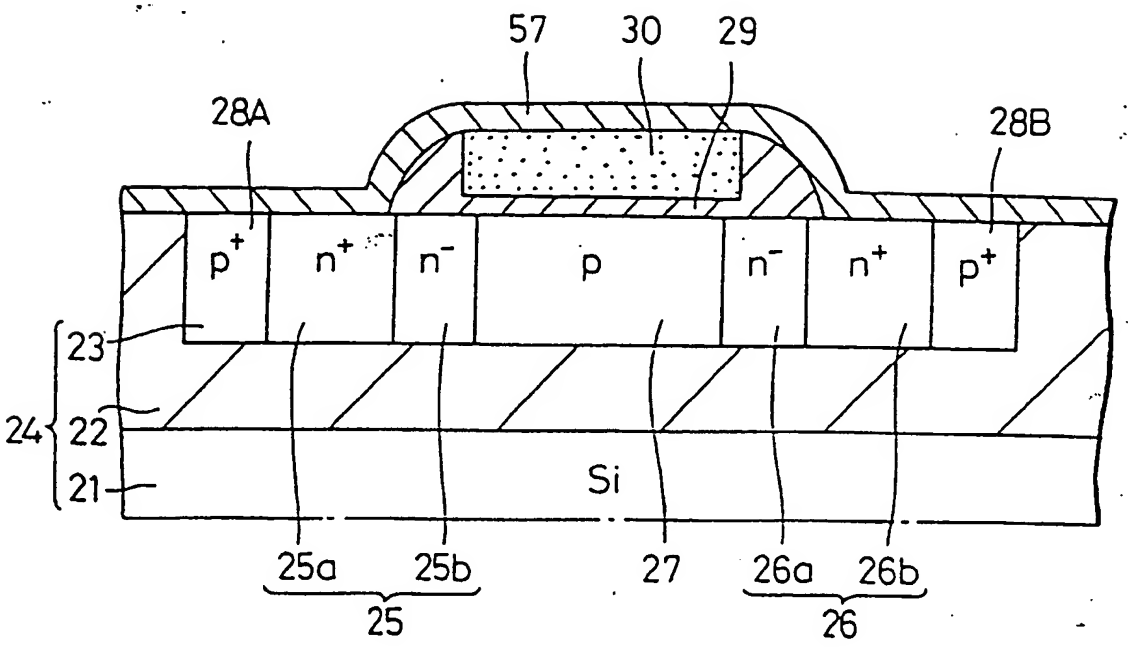
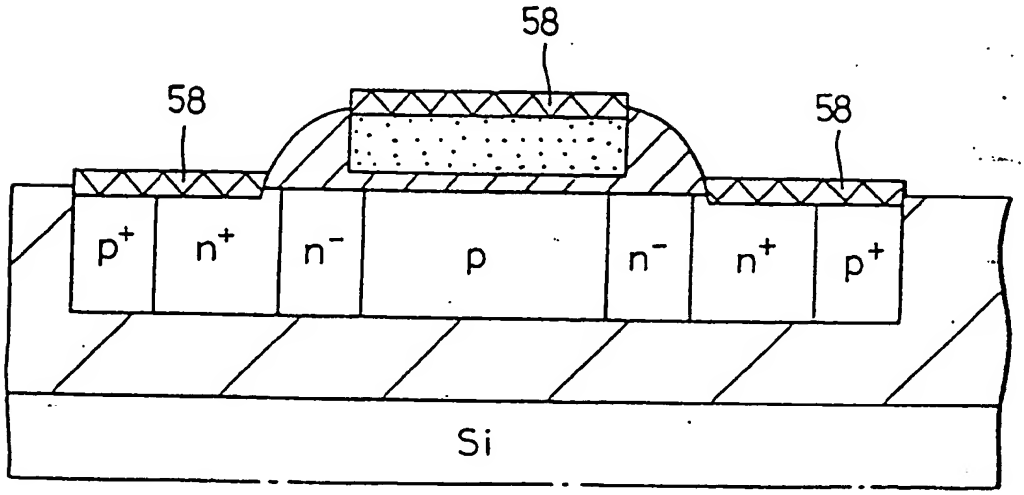



FIG. 29B



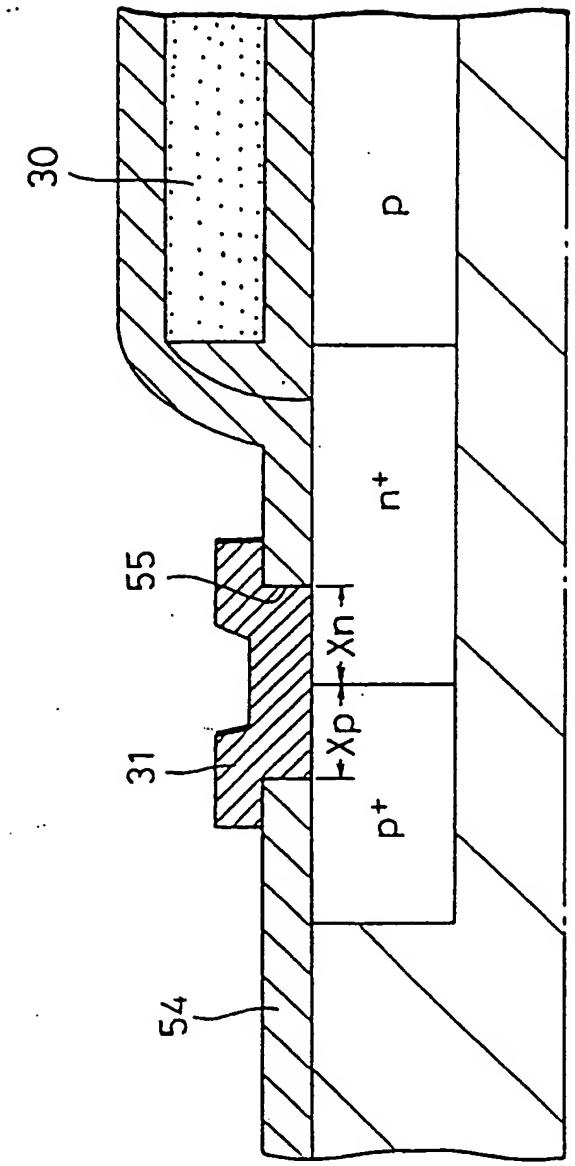



FIG. 30

FIG. 32

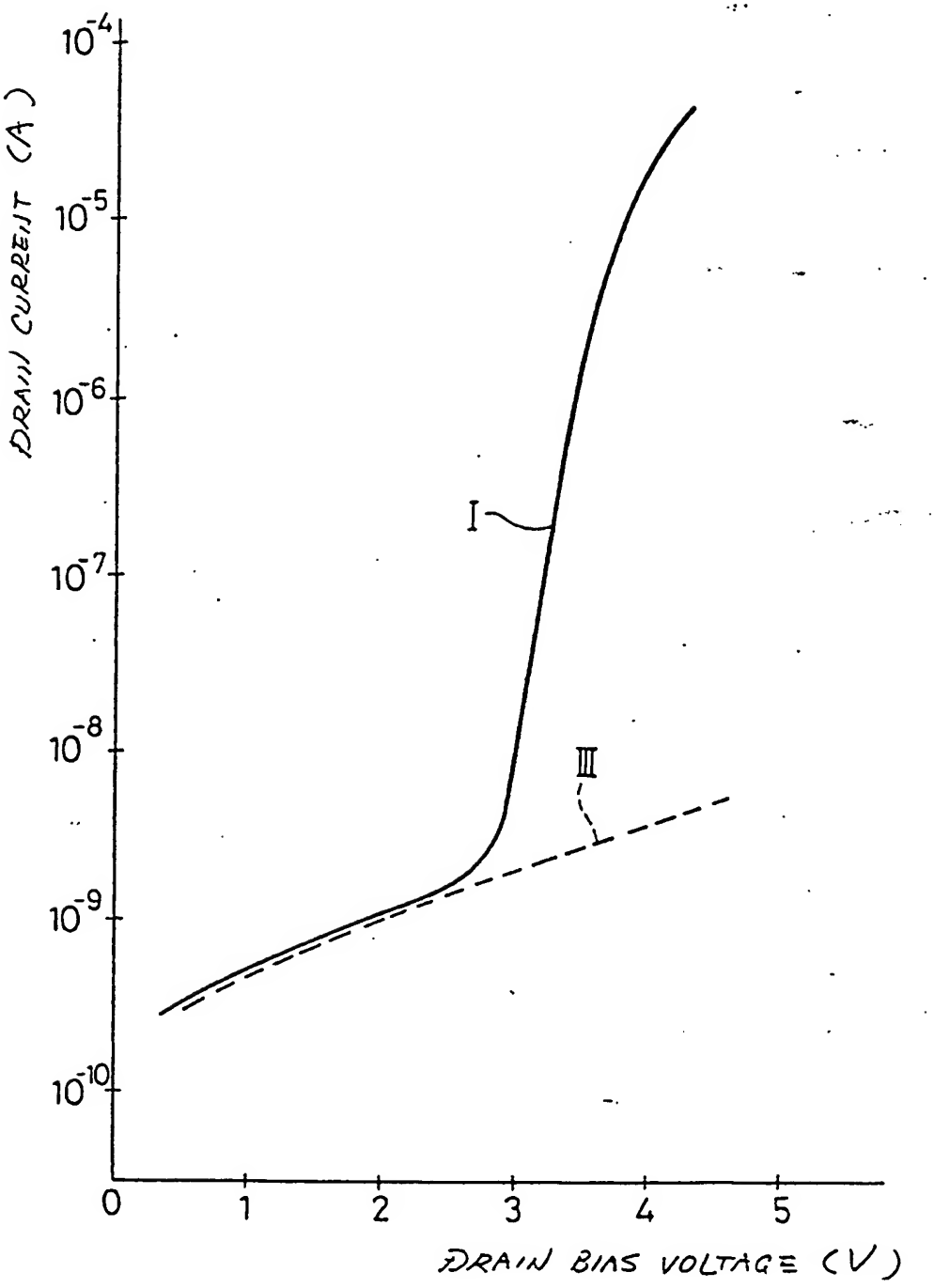

DRAIN CURRENT (A)
$10^{-4}$
$10^{-5}$
$10^{-6}$
$10^{-7}$
$10^{-8}$
$10^{-9}$
$10^{-10}$
I
III
0
1
2
3
4
5
DRAIN BIAS VOLTAGE (V)

FIG. 34A

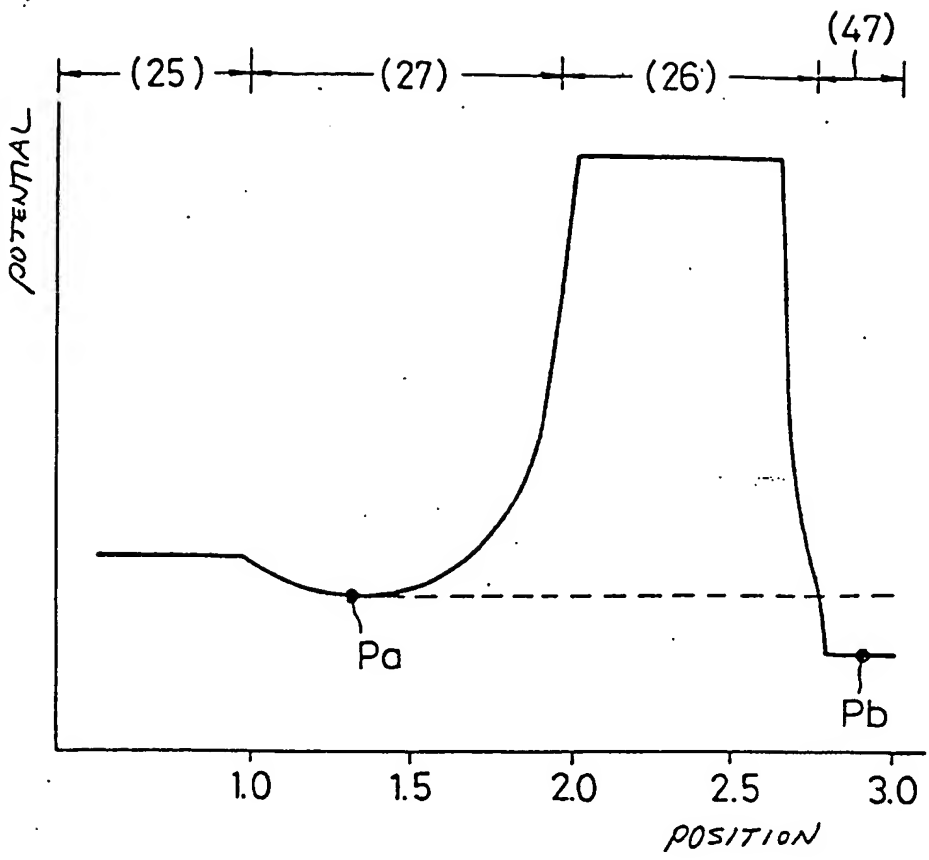



FIG. 34B

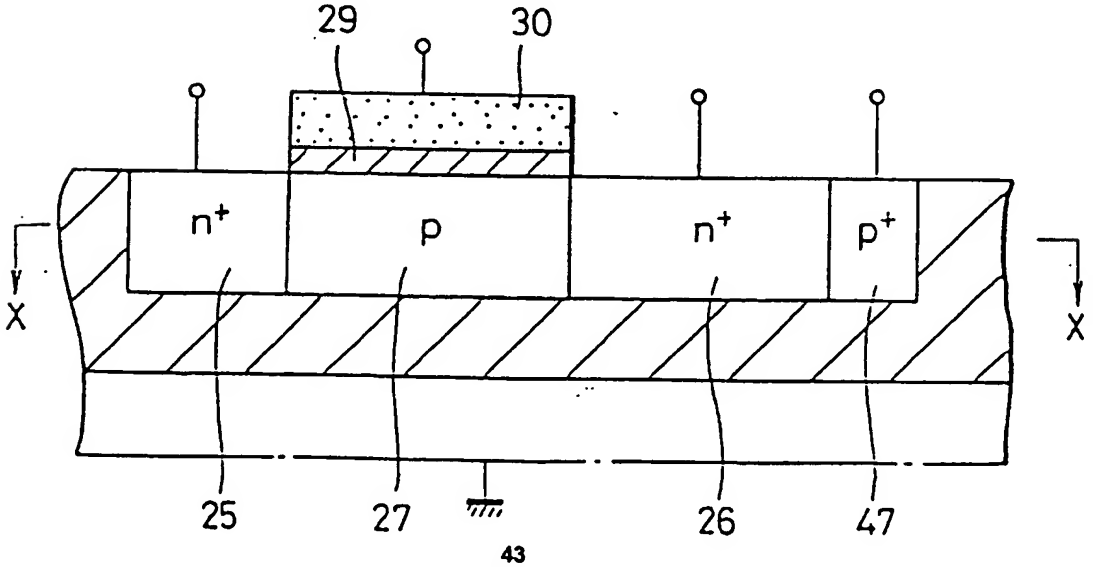


FIG. 38A

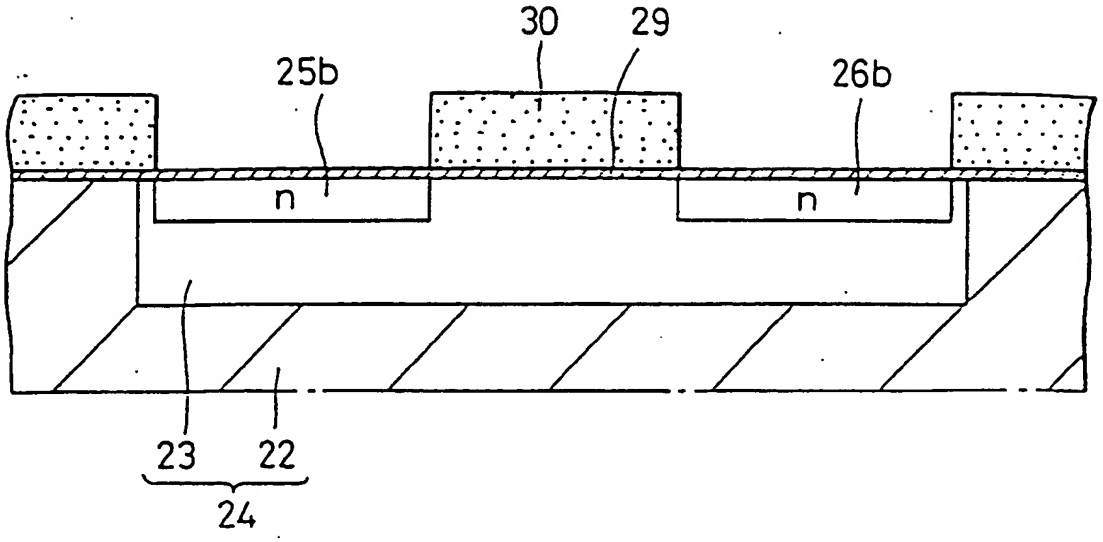



FIG. 38B

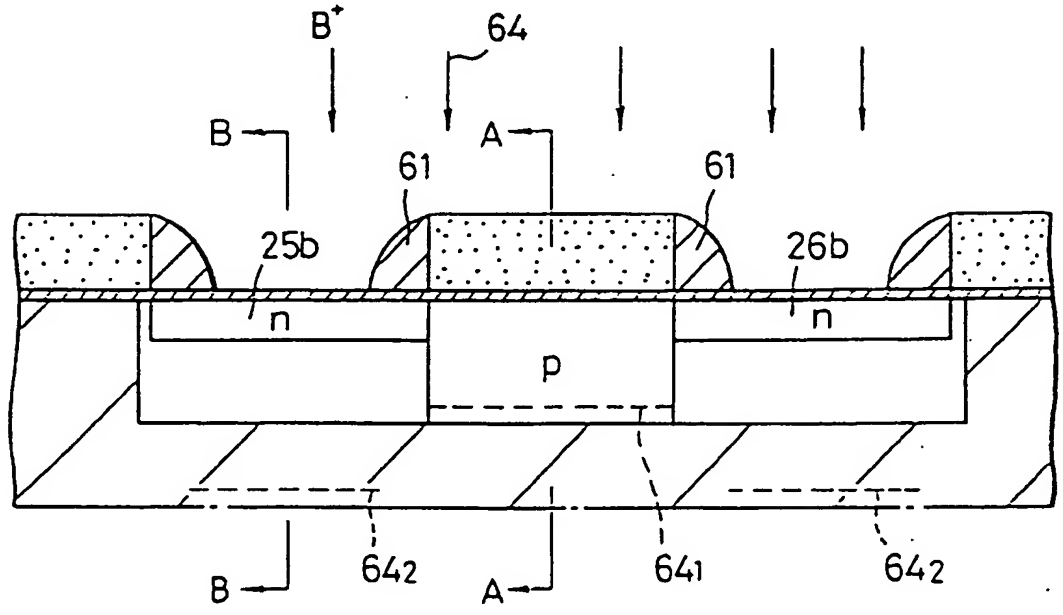


FIG. 39A

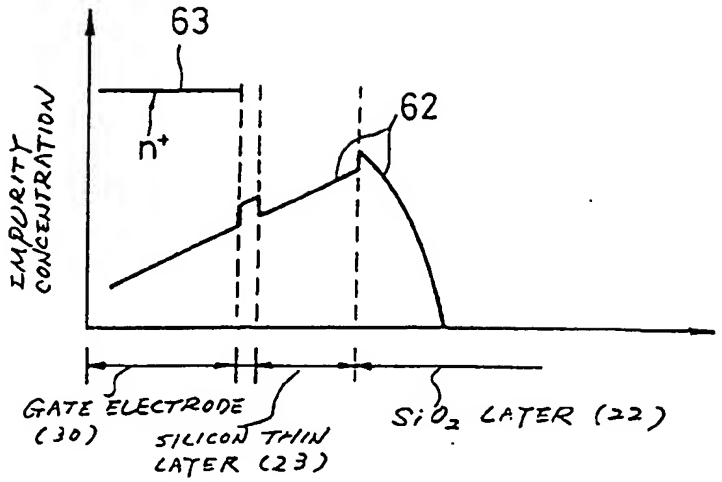



FIG. 39B

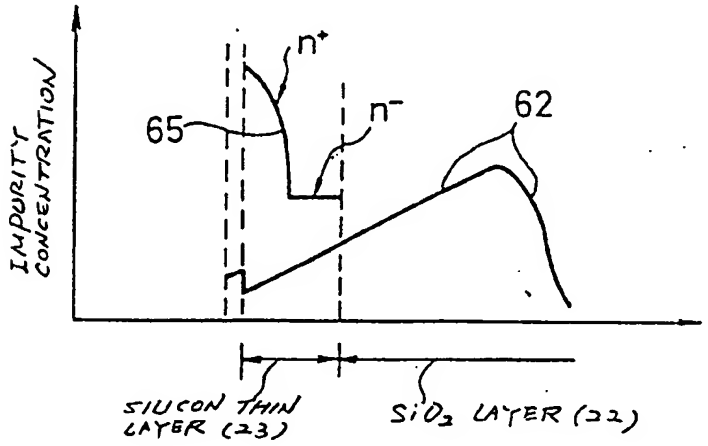



FIG. 40

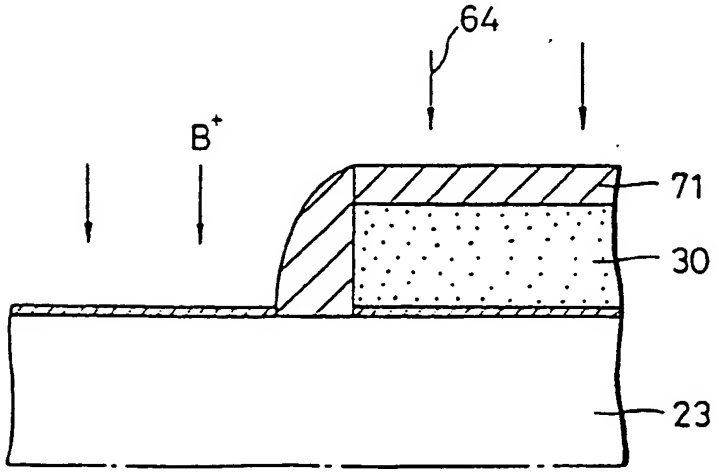


FIG. 41D

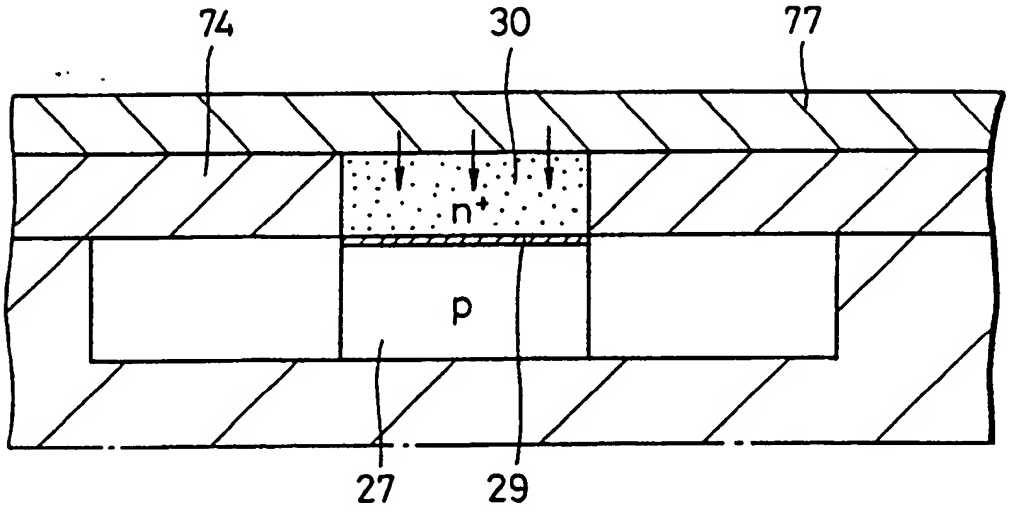



FIG. 41E

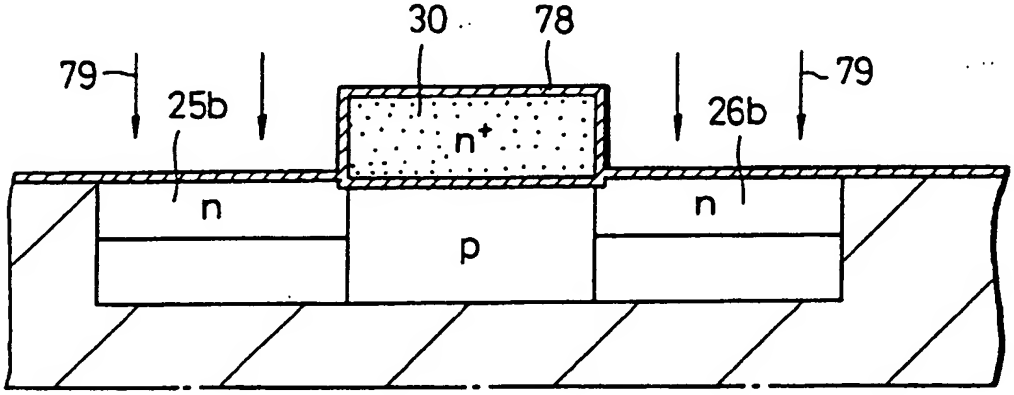



FIG. 41F